WHAT IS CLAIMED IS:

1. A semiconductor switch core comprising:

a buffer matrix having one buffer memory per crosspoint to which cells having differing priority classes are written;

a high priority signaling element associated with a corresponding crosspoint, the high priority signaling element when active indicating that a high priority cell is in a queue awaiting writing to the buffer memory for its corresponding crosspoint;

input/output logic for reading out any low priority cell that resides in the buffer memory for the corresponding crosspoint when the high priority signaling element is active.

2. The apparatus of claim 1, wherein the high priority signaling element is also active when the high priority cell is in the buffer memory for the corresponding crosspoint.

3. The apparatus of claim 1, wherein the buffer matrix has only one buffer memory per crosspoint.

4. The apparatus of claim 1, wherein the semiconductor switch core has a plurality of ports, and wherein the low priority cell read out from the buffer memory for the corresponding crosspoint when the high priority signaling element is active is applied to a port of the switch for transmission out of the switch.

5. The apparatus of claim 1, further comprising a low priority signaling element associated with a corresponding crosspoint, the low priority signaling element when active indicating that a low priority cell is in the buffer memory for the corresponding crosspoint so long as no high priority cell is in a queue awaiting writing to the buffer memory for the corresponding crosspoint.

6. The apparatus of claim 1, wherein the high priority signaling element is a semiconductor memory element.

7. A switching node of a telecommunications system comprising:

a semiconductor switch core comprising:

a buffer matrix having one buffer memory per crosspoint to which cells having differing priority classes are written;

plural switch core ports, each of the switch core ports writing cells to a row of the matrix and reading cells from a column of the matrix;

a high priority signaling element associated with a corresponding crosspoint;

plural switch port devices connected to corresponding ones of the plural switch core ports, an appropriate one of the switch port devices comprising a queue for low priority cells awaiting writing to the corresponding crosspoint and a queue for high priority cells awaiting writing to the corresponding crosspoint; and

wherein the high priority signaling element when active indicates that a high priority cell is in the queue for high priority cells awaiting writing to the buffer memory for its corresponding crosspoint, and wherein an appropriate one of the switch core ports reads out any low priority cell that resides in the buffer memory for the corresponding crosspoint when the high priority signaling element is active.

8. The apparatus of claim 7, wherein the high priority signaling element is also active when the high priority cell is in the buffer memory for the corresponding crosspoint.

9. The apparatus of claim 7, wherein the buffer matrix has only one buffer memory per crosspoint.

10. The apparatus of claim 7, wherein the low priority cell read out from the buffer memory for the corresponding crosspoint when the high priority signaling element is active is applied to the appropriate one of the switch core ports for transmission out of the switch.

11. The apparatus of claim 7, further comprising a low priority signaling element associated with a corresponding crosspoint, the low priority signaling element when active indicating that a low priority cell is in the buffer memory for the

corresponding crosspoint so long as no high priority cell is in the high priority queue awaiting writing to the buffer memory for the corresponding crosspoint.

12. The apparatus of claim 7, wherein the high priority signaling element is a semiconductor memory element.

13. A method of operating a semiconductor switch core, the semiconductor switch core comprising a buffer matrix having one buffer memory per crosspoint, a high priority signaling element associated with a corresponding crosspoint; and an input/output logic for reading out cells from the corresponding crosspoint; wherein the method comprises:

writing a low priority cell to the buffer memory for the corresponding crosspoint;

activating the high priority signaling element when a high priority cell is in a queue awaiting writing to the buffer memory for the corresponding crosspoint;

reading out the low priority cell from the buffer memory for the corresponding crosspoint when the high priority signaling element is active.

14. The method of claim 13, further comprising writing the high priority cell to the buffer memory for the corresponding crosspoint after the low priority cell has been read out.

15. The method of claim 13, further comprising activating the high priority signaling element also when the high priority cell is in the buffer memory for the corresponding crosspoint.

16. The method of claim 15, further comprising activating a low priority signaling element when a low priority cell is in the buffer memory for the corresponding crosspoint so long as no high priority cell is in a queue awaiting writing to the buffer memory for the corresponding crosspoint.

17. The method of claim 15, wherein the step of activating the high priority signaling element involves writing a predetermined value to a semiconductor memory element comprising the switch core.

18. A method of operating a semiconductor switching node, the semiconductor switch core comprising a semiconductor switch core and plural switch port devices, the semiconductor switch core comprising a buffer matrix having one buffer memory per crosspoint, plural switch core ports, and a high priority signaling element associated with a corresponding crosspoint, the plural switch port devices being connected to corresponding ones of the plural switch core ports, the method comprising:

in an appropriate one of the switch port devices, queuing in a queue for low priority cells a low priority cell awaiting writing to the corresponding crosspoint;

writing the low priority cell to the buffer memory for the corresponding crosspoint;

in the appropriate one of the switch port devices, queuing in a queue for high priority cells a high priority cell awaiting writing to the corresponding crosspoint;

activating the high priority signaling element when the high priority cell is queued in queue for high priority cells;

reading out the low priority cell from the buffer memory for the corresponding crosspoint when the high priority signaling element is activated.

19. The method of claim 18, further comprising writing the high priority cell to the buffer memory for the corresponding crosspoint after the low priority cell has been read out.

20. The method of claim 18, further comprising activating the high priority signaling element also when the high priority cell is in the buffer memory for the corresponding crosspoint.

21. The method of claim 18, further comprising activating a low priority signaling element when a low priority cell is in the buffer memory for the corresponding crosspoint so long as no high priority cell is in a queue awaiting writing to the buffer memory for the corresponding crosspoint.

22. The method of claim 18, wherein the step of activating the high priority signaling element involves writing a predetermined value to a semiconductor memory element comprising the switch core.

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